Q. Code: 575034

B.E./B.TECH. Degree Examination, December 2020

Fourth Semester

CS16404 -Computer Architecture

(Regulation 2016)

Time: Three hours Maximum : 80 Marks

Answer **ALL** questions

PART A - (8 X 2 = 16 marks)

1. Statement I: The set of instructions issued together in one clock cycle is issue slot.

   Statement II: The packet may be determined statically by the compiler or dynamically by the processor.

   a. Statement I and II are correct
   b. Statement I and II are incorrect
   c. Statement I is correct and Statement II is incorrect
   d. Statement I is incorrect and Statement II is correct

2. Match the following

   1. Von Neumann architecture
   2. Fault tolerance
   3. Distributed systems
   4. Array processor

   With

   A. MIMD
   B. SISD
   C. SIMD
   D. MISD

   a. 1-B, 2-D, 3-A, 4-C
   b. 1-C, 2-D, 3-A, 4-B
   c. 1-B, 2-A, 3-D, 4-C
   d. 1-B, 2-D, 3-C, 4-A

3. An abstract view of MIPS implementation having major functional unit is in the order of

   a. PC, ALU, Instruction memory, Register file, Data memory
   b. PC, Instruction memory, Register file, Data memory, ALU
   c. PC, ALU, Instruction memory, Register file, Data memory
   d. PC, Instruction memory, Register file, ALU, Data memory

4. In _____ mapping, the data can be mapped anywhere in the Cache Memory.
   a) Associative
   b) Direct
   c) Set Associative
   d) Indirect
5. Convert the given decimal number into binary and Express it in IEEE 754 Single Precision Format $(17.250)_{d}$.
6. Analyze the characteristics of SMT processor.
7. Mention the control signals and control word needed to execute branch instruction.
8. Integrate the ideas of in-order execution and out-of-order execution.

PART B - (4 X16 = 64 marks)

09. (a) (i) Assume that the variables 'f' and 'g' are assigned to registers $S0 and $S1 respectively. Assume that the base address of the array 'A' is in register $S2. Assume 'f' is zero initially. **(8)**

```
f = g - A[4];
A[5] = f + 100;
```

Translate the above 'C' statements into MIPS code. Represent the same MIPS code in Machine Language.

(ii) Examine the following sequence of instructions and identify the addressing modes used and the operation done in every instruction **(8)**

```
lui $s0,61
add$S1,$S2,$S3
J 2500
bne $s2,$s3,loop
```

(OR)

(b) The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power. The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power **(16)**

(i) For each processor find the average capacitive loads

(ii)Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.

(iii) If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current.

Note: power is defined as the product of voltage and current

10. (a) Multiply the numbers 0.125 and 0.423 in binary using floating point Multiplication Algorithm. Add suitable comments to each step along with its flowchart. **(16)**

(OR)

(b) Divide the $(8)_{10}$ by $(5)_{10}$ using division algorithm and explain the algorithm with relevant diagrams. **(16)**

11. (a) Design a datapath with control unit and implement it for R type instruction. **(16)**

(OR)

(b) Design and develop working of an instruction pipeline under various situations of pipeline stalls. **(16)**

12. (a) Consider a direct mapped cache memory organization in which main memory consists of 4096 blocks and cache memory consists of 512 blocks. Each block consists of 18 words. **(16)**

    a. What is the size of main memory?
    b. What is the size of cache memory?
    c. How many address lines are needed for addressing main memory?
    d. What is the size of word, block ad tag fields?

(OR)

(b) Analyze the implementation of virtual memory organization in detail **(16)**